EDP-CM-LPC1343 Command Module
User Manual

Version 1.03

5th August 2010

Contents

1. Introduction

The RS-EDP platform is a system, has been designed to utilise many different manufacturers' microprocessors. To support NXP range or ARM/Cortex MCU's a single Command Module (CM) has been designed to accommodate four different device types. These are LPC2368 (ARM7), LPC1768 (Cortex M3), LPC1343 (Cortex M3) and LPC1113 (Cortex M0).

Each of the boards comes with its own suite of software to fully exercise the RS-EDP Application Modules and the peripherals available on the MCU device.

In an RS-EDP system there is usually one Command Module / CPU Module (CM) and one or more Applications Modules (AM) plugged in to the Base Board (BB). These NXP modules have been designed as the Command Module for the system.

The 'Command Module' in a system dictates whether the whole system is a 3.3V one or a 5.0V one. All of these modules use a 3.3V microprocessor and consequently the I/O is mostly 3.3V also.
To tell the rest of the system the Command Module is a 3.3V one not a 5.0V one, the Vcc_CM line on the base board is connected to 3.3V by the tracking on the Command Module board. This Vcc_CM is used as a reference by the other modules, such as the analogue module, to limit the output voltage to 3.3V. The command voltage line is also used by the #RESET circuit, as the voltage reference to pull up to after the reset line has been asserted low.

The RS-EDP-CM-NXP module maps the I/O of the MCU on the board to the backplane of the RS-EDP system. As there are quite a few dual function pins on the NXP processors and hence several link options have been made to accommodate the various options the user may wish to use. Extensive use of the I2C capability is used to communicate to the application modules in the system.

2. Pin Allocation

2.1 Allocation of MCU pins to backplane functions

The CM has been mapped to the backplane to maximise the functionality of the system and the AMs. A document called a Pin Allocation spreadsheet exists which details the mapping of the pins to the backplane. The details of this mapping are detailed below.

Below are detailed the pin number of the MCU, the pin name, a comment on its usage and the signals name to which it is allocated on the backplane.
As the same PCB is used for variants of LPC processor some of the mapping may appear a little strange. For example this device has no CAN but is allocated some CAN resource on the backplane. This is because other NXP variants do have a CAN controller on board and the mapping is done to accommodate this other device.

LPC1343FBD48		Comment	RS-EDP-BASE BOARD

Pin	Name of function used on PIC		Name
34 & 28	TDO/PIO1_1/AD2/CT32B1_MAT0 & PIO0_9/MOSI/CT16B0_MAT1/SWO	JTAG interface on LPC module	
32	TDI/PIO0_11/ADC0/CT32B0/MAT3	JTAG interface on LPC module	
33 & 39	TMS/PIO1_0/AD1/CT32B1_CAP0 & SWDIO/PIO1_3/AD4/CT32B1_MAT2	JTAG interface on LPC module	
35	TRST/PIO1_2/AD3/CT32B1_MAT1	JTAG interface on LPC module	
29	SWCLK/PIO0_10/SCK/CT16B0_MAT2	JTAG interface on LPC module	
40	PIO1_4/AD5/CT32B1_MAT3/WAKEUP	2 link options	AN0
		2 link options	AN8
3	#RESET/PIO0_0		#RESIN
42	PIO1_11/AD7	2 link options	AN4
		2 link options	AN12
6	XTALIN	Xtal on module	
7	XTALOUT	Xtal on module	
15	PIO0_4/SCL		CNTRL_I2C_SCL
16	PIO0_5/SDA		CNTRL_I2C_SDA
1	PIO2_6		EVG1_GPIO42
4	PIO0_1/CLKOUT/CT32B0_MAT2/USB_FTOGGLE	2 link options	EVG0_GPIO40
		2 Link options - User LED1	
8	VDDIO		3.3V
20	USB_DP		USB_DEV_D+
19	USB_DM		USB_DEV_D-
5	VSSIO		SGND
30	PIO1_10/AD6/CT16B1_MAT1	3 link options	EVG5_GPIO50
		3 link options	EVG8_GPIO56
		3 link options	EVG0_GPIO40
36	PIO3_0	2 link options	MOTORP0H
		2 link options	EVG9_GPIO57
37	PIO3_1	2 link options	MOTORH0_ENC0
		2 link options	EVG10_GPIO58
38	PIO2_3/#RI	2 link options	EMG_TRAP
		2 link options	EVG11_GPIO59
43	PIO3_2	2 link options	MOTORP0L
		2 link options	EVG12_GPIO60
48	PIO3_3	2 link options	MOTORH1_ENC1
		2 link options	EVG13_GPIO61
41	VSSIO		SGND
44	VDDCORE		3.3V
45	PIO1_5/#RTS/CT32B0_CAP0		EVM5_GPIO47
10	PIO0_2/SSEL/CT16B0_CAP0	2 link options	MOTORP2H
		2 link options	EVG17_GPIO65
27	PIO0_8/MISO/CT16B0_MAT0	2 link options	MOTORP2L
		2 link options	EVG18_GPIO66

2	PIO2_0/#DTR	2 link options	GPIO0
		2 link options	EVG6_GPIO52
31	PIO2_11/SCK	2 link options	GPIO1
		2 link options	EVG7_GPIO54
13	PIO2_1/#DSR	2 link options	ASC1_TX_TTL_ASC0_DTR
		2 link options	CAN1_RX
26	PIO2_2/#DCD	2 link option	EVG4_GPIO48
		2 link option	EVG19_GPIO67
25	PIO2_10	2 link option	CPU_DAC01_GPIO19
		2 link option	EVG3_GPIO46
24	PIO2_9	2 link option	CPU_DACO0_GPIO17
		2 link option	EVG2_GPIO44
23	PIO0_7/#CTS		EVM9_GPIO55
22	PIO0_6/#USB_CONNECT/SCK	2 link options	ASC1_RX_TTL
		2 Link options	EVM8_GPIO53
12	PIO2_8	2 link options	ASC1_TX_TTL
		2 Link options	EVM7_GPIO51
21	PIO2_5	2 Link options	EVM6_GPIO49
		2 Link options	GPIO2_MCIDAT0
9	PIO1_8/CT16B1_CAP0	2 Link options	EVM4_GPIO45
		2 Link options	GPIO14_MCIPWR
18	PIO2_4	2 Link options	EVM3_GPIO43
		2 Link options	GPIO12_MCICMD
11	PIO2_7	2 Link options	EVM2_GPIO41_CAPADC
		2 Link options	GPIO10_MCICLK
17	PIO1_9/CT16B1_MAT0	3 link options	GPIO9_I2S_RX_WS
		3 link options	EVM1_GPIO23
		3 link options	CPU_DACO0_GPIO17
14	PIO0_3/USB_VBUS	2 link option	GPIO7_I2S_RX_CLK
		2 Link options	EVM0_GPIO21
47	PIO1_7/TXD/CT32B0_MAT1	3 Link options	ASC0_TX_TTL
		3 link options	AN7
		3 link options	AN15
46	PIO1_6/RXD/CT32B0_MAT0	3 Link options	ASC0_RX_TTL
		3 link options	AN6
		3 link options	AN14

2.2 Resources Used/Available by LPC1343

Resources Used/Available
3.3V
SGND
#RESIN
AN0
AN4
AN6
AN7
AN8
AN12
AN14
AN15
ASC0_TX_TTL
ASC0_RX_TTL
ASC1_TX_TTL
ASC1_RX_TTL
ASC1_TX_TTL_ASC0_DTR
CAN1_RX
CNTRL_I2C_SCL
CNTRL_I2C_SDA
CPU_DACO0_GPIO17
CPU_DAC01_GPIO19
EVG0_GPIO40
EVG1_GPIO42
EVG2_GPIO44
EVG3_GPIO46
EVG4_GPIO48
EVG5_GPIO50
EVG6_GPIO52
EVG7_GPIO54
EVG8_GPIO56
EVG9_GPIO57
EVG10_GPIO58
EVG11_GPIO59
EVG12_GPIO60
EVG13_GPIO61
EVG17_GPIO65
EVG18_GPIO66
EVG19_GPIO67
EVM0_GPIO21
EVM1_GPIO23
EVM2_GPIO41_CAPADC
EVM3_GPIO43
EVM4_GPIO45
EVM5_GPIO47
EVM6_GPIO49
EVM7_GPIO51
EVM8_GPIO53
EVM9_GPIO55
GPIO0
GPIO1
GPIO2_MCIDAT0
GPIO7_I2S_RX_CLK
GPIO9_I2S_RX_WS
GPIO10_MCICLK
GPIO12_MCICMD
GPIO14_MCIPWR
MOTORP0H
MOTORP0L

MOTORH0_ENC0
MOTORH1_ENC1
MOTORP2H
MOTORP2L
EMG_TRAP
USB_DEV_D+
USB_DEV_D-
Local User LED1

2.3 Alphabetical Listing of MCU Pins

Pin	Alphabetic Listing of Available I/O
3	#RESET/PIO0_0
4	PIO0_1/CLKOUT/CT32B0_MAT2/USB_FTOGGLE
10	PIO0_2/SSEL/CT16B0_CAP0
14	PIO0_3/USB_VBUS
15	PIO0_4/SCL
16	PIO0_5/SDA
22	PIO0_6/#USB_CONNECT/SCK
23	PIO0_7/#CTS
27	PIO0_8/MISO/CT16B0_MAT0
40	PIO1_4/AD5/CT32B1_MAT3/WAKEUP
45	PIO1_5/#RTS/CT32B0_CAP0
46	PIO1_6/RXD/CT32B0_MAT0
47	PIO1_7/TXD/CT32B0_MAT1
9	PIO1_8/CT16B1_CAP0
17	PIO1_9/CT16B1_MAT0
30	PIO1_10/AD6/CT16B1_MAT1
42	PIO1_11/AD7
2	PIO2_0/#DTR
13	PIO2_1/#DSR
26	PIO2_2/#DCD
38	PIO2_3/#RI
18	PIO2_4
21	PIO2_5
1	PIO2_6
11	PIO2_7
12	PIO2_8
24	PIO2_9
25	PIO2_10
31	PIO2_11/SCK
36	PIO3_0
37	PIO3_1
43	PIO3_2
48	PIO3_3
29	SWCLK/PIO0_10/SCK/CT16B0_MAT2
32	TDI/PIO0_11/ADC0/CT32B0/MAT3
34 & 28	TDO/PIO1_1/AD2/CT32B1_MAT0 & PIO0_9/MOSI/CT16B0_MAT1/SWO
33 & 39	TMS/PIO1_0/AD1/CT32B1_CAP0 & SWDIO/PIO1_3/AD4/CT32B1_MAT2
35	TRST/PIO1_2/AD3/CT32B1_MAT1
19	USB_DM
20	USB_DP
44	VDDCORE
8	VDDIO
5	VSSIO
41	VSSIO
6	XTALIN
7	XTALOUT

2.4 Backplane - Base Board Signals

Base Board Signal Name	EDPCON1	EDPCON2	Break Out Connector	
#CS0		53 & 54		
#CS1		55 & 56		
#CS2		57 & 58		
#CS3		59 & 60		
#PSEN		51 & 52		
#RD		45 & 46		
#RESIN		1 & 2	P603	26
#RESOUT		3 & 4	P603	27
#WR		47 & 48		
#WRH		49 & 50		
12V	133		P603	47
12V	134		P603	47
12V	135		P603	47
12V	136		P603	47
12V GND	137		P603	48
12V GND	138		P603	48
12V GND	139		P603	48
12V GND	140		P603	48
3.3V	127		P603	44
3.3V	128		P603	44
3.3V		95 & 96	P603	44
3V BAT	124		P603	42
5.0V	129		P603	45
5.0V	130		P603	45
5.0V		97 & 98	P603	45
A0_AD0		41 & 42		
A1_AD1		39 & 40		
A2_AD2		37 & 38		
A3_AD3		35 & 36		
A4_AD4		33 & 34		
A5_AD5		31 & 32		
A6_AD6		29 & 30		
A7_AD7		27 & 28		
A8_AD8		25 & 26		
A9_AD9		23 & 24		
A10_AD10		21 & 22		
A11_AD11		19 & 20		
A12_AD12		17 & 18		
A13_AD13		15 & 16		
A14_AD14		13 & 14		
A15_AD15		11 & 12		
ALE		43 & 44		
AN_REF	1		P601	6
AN0	3		P603	2
AN1	4		P603	6
AN2	5		P603	1
AN3	6		P603	5
AN4	7		P602	2
AN5	8		P602	4
AN6	9		P602	1
AN7	10		P602	3
AN8	11		P601	2
AN9	12		P601	4
AN10	13		P601	1
AN11	14		P601	3

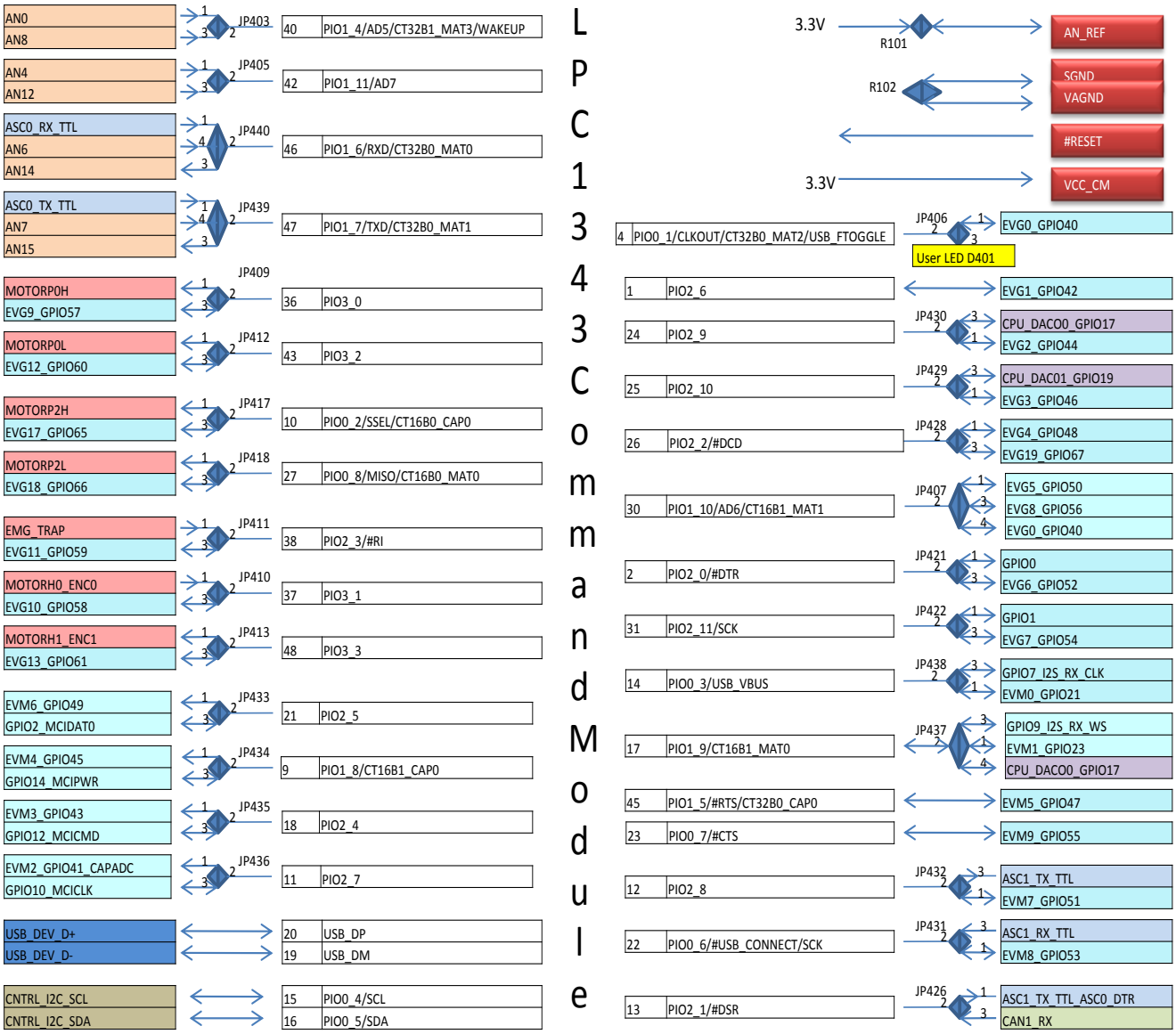
AN12	15		P603	4
AN13	16		P602	6
AN14	17		P603	3
AN15	18		P602	5
ASC0_RX_TTL	89		P602	30
ASC0_TX_TTL	91		P602	31
ASC1_RX_TTL	93		P602	32
ASC1_RX_TTL_ASC0_DSR	99		P602	35
ASC1_TX_TTL	95		P602	33
ASC1_TX_TTL_ASC0_DTR	97		P602	34
CAN0_RX		61 & 62		
CAN0_TX		63 &64		
CAN1_RX	121		P602	46
CAN1_TX	123		P602	47
CANH0		89 & 90	P603	40
CANL0		91 & 92	P603	41
CNTRL_I2C_SCL		79 & 80	P603	35
CNTRL_I2C_SDA		77 & 78	P603	34
CNTRL_SPI_#CS_NSS		75 & 76	P603	33
CNTRL_SPI_CLK		69 & 70	P603	30
CNTRL_SPI_MRST		71 & 72	P603	31
CNTRL_SPI_MTSR		73 & 74	P603	32
CPU_DACO0_GPIO17	38		P603	7
CPU_DACO1_GPIO19	40		P601	7
EMG_TRAP	114		P601	44
ETH_LNK_LED	111		P602	41
ETH_RX-	109		P602	40
ETH_RX_LED	113		P602	42
ETH_RX+	107		P602	39
ETH_SPD_LED	115		P602	43
ETH_TX-	105		P602	38
ETH_TX+	103		P602	37
EVG0_GPIO40	61		P602	16
EVG1_GPIO42	63		P602	17
EVG2_GPIO44	65		P602	18
EVG3_GPIO46	67		P602	19
EVG4_GPIO48	69		P602	20
EVG5_GPIO50	71		P602	21
EVG6_GPIO52	73		P602	22
EVG7_GPIO54	75		P602	23
EVG8_GPIO56	77		P602	24
EVG9_GPIO57	78		P601	26
EVG10_GPIO58	79		P602	25
EVG11_GPIO59	80		P601	27
EVG12_GPIO60	81		P602	26
EVG13_GPIO61	82		P601	28
EVG14_GPIO62	83		P602	27
EVG15_GPIO63	84		P601	29
EVG16_GPIO64	85		P602	28
EVG17_GPIO65	86		P601	30
EVG18_GPIO66	87		P602	29
EVG19_GPIO67	88		P601	31
EVG20_GPIO69_ASCO_RTS	92		P601	33
EVM0_GPIO21	42		P601	8
EVM1_GPIO23	44		P601	9
EVM2_GPIO41_CAPADC	62		P601	18
EVM3_GPIO43	64		P601	19
EVM4_GPIO45	66		P601	20
EVM5_GPIO47	68		P601	21
EVM6_GPIO49	70		P601	22
EVM7_GPIO51	72		P601	23

EVM8_GPIO53	74		P601	24
EVM9_GPIO55	76		P601	25
EVM10_GPIO68_ASCO_CTS	90		P601	32
GPIO0	21		P603	13
GPIO1	22		P603	15
GPIO2_MCI_DAT0	23		P603	14
GPIO3	24		P603	16
GPIO4_MCI_DAT1	25		P603	17
GPIO5_I2S_TX_WS	26		P603	19
GPIO6_MCI_DAT2	27		P603	18
GPIO7_I2S_RX_CLK	28		P603	20
GPIO8_MCI_DAT3	29		P603	22
GPIO9_I2S_RX_WS	30		P603	21
GPIO10_MCI_CLK	31		P603	23
GPIO11_I2S_RX_SDA	32		P603	24
GPIO12_MCI_CMD	33			
GPIO13_I2S_TX_CLK	34		P603	25
GPIO14_MCI_PWR	35		P603	12
GPIO15_I2S_TX_SDA	36		P603	8
GPIO24_AD7	45		P602	8
GPIO25_AD15	46		P601	10
GPIO26_AD6	47		P602	9
GPIO27_AD14	48		P601	11
GPIO28_AD5	49		P602	10
GPIO29_AD13	50		P601	12
GPIO30_AD4	51		P602	11
GPIO31_ADI2	52		P601	13
GPIO32_AD3	53		P602	12
GPIO33_AD11	54		P601	14
GPIO34_AD2	55		P602	13
GPIO35_AD10	56		P601	15
GPIO36_AD1	57		P602	14
GPIO37_AD9	58		P601	16
GPIO38_AD0	59		P602	15
GPIO39_AD8	60		P601	17
I2C_GEN0_SCL		7 & 8	P603	29
I2C_GEN0_SDA		5 & 6	P603	28
I2C_GEN1_SCL	119		P602	45
I2C_GEN1_SDA	117		P602	44
IRQ_GPIO16_CNTRL_I2C_INT	37		P603	11
IRQ_GPIO18_I2C_GEN0_INT	39		P603	10
IRQ_GPIO20_I2C_GEN1_INT	41		P603	9
IRQ_GPIO22_I2C_INT	43		P602	7
MOTOR_TCO_FB	122		P601	48
MOTORH0_ENC0	116		P601	45
MOTORH1_ENC1	118		P601	46
MOTORH2_ENC2	120		P601	47
MOTORP0H	102		P601	38
MOTORP0L	100		P601	37
MOTORP1H	106		P601	40
MOTORP1L	104		P601	39
MOTORP2H	110		P601	42
MOTORP2L	108		P601	41
MOTORPWM	112		P601	43
SGND	131		P603	46
SGND	132		P603	46
SGND		9 & 10	P603	46
SGND		99 & 100	P603	46
SPI_SSC_#CS_NSS	101		P602	36
SPI_SSC_CLK	98		P601	36
SPI_SSC_MRST_MISO	94		P601	34

SPI_SSC_MTSR_MOSI	96		P601	35
USB_DEBUG_D-		67 & 68		
USB_DEBUG_D+		65 & 66		
USB_DEV_D-		87 & 88	P603	39
USB_DEV_D+		85 & 86	P603	38
USB_HOST_D-		83 & 84	P603	37
USB_HOST_D+		81 & 82	P603	36
VAGND	19		P601	5
VAGND	20		P601	5
Vcc_CM	125		P603	43
Vcc_CM	126		P603	43
Vcc_CM		93 & 94	P603	43

Note: This spread sheet is derived from the Pin Allocation Spreadsheet for this CPU Module.
The user manual for the base board also contains details of the back plane signals and the pin outs.

2.5 Mapping Aid



3. Solder Link Options

Many of the options for the Command Module board require a solder bridge to be made or a track to be cut. The CM board has been designed to be configured in the most popular setting by using a small track between the options, which will require cutting with a sharp knife before making the alternate connection options.

A documents called a Mapping Aid exist to help explain the resources available on the MCU and how it can interface with the other modules within the system.

The options we have are as follows:

VDDA

JP201 (1-2)	VDDA on the MCU is connected to 3.3V
JP201 (2-3)	VDDA on the MCU is connected to AN_REF on the backplane

VDDA is the power supply voltage to the on board ADC circuitry. Using a lower noise AN_REF signal will yield better results. The AN_REF signal is usually provided by a stable voltage reference source present on the Analogue Module.

Vref

JP202 (1-2)	VREF on the MCU is connected to 3.3V
JP202 (2-3)	VREF on the MCU is connected to AN_REF on the backplane

This is the voltage reference that is used to measure the analogue input voltages against. An AN_REF signal will provide better results than the 3.3V signal. The AN_REF signal is usually provided by a stable voltage reference source present on the Analogue Module.

VBAT

JP203 (1-2)	VBAT on the MCU is connected to 3.3V
JP203 (2-3)	VREF on the MCU is connected to 3V3_BATT on the backplane

This option is irrelevant as the LPC1343 does not a VBAT terminal. This jumper is provided for the LPC1768/LPC2368 variants of the Command Module.

Port PI00 Options

PIO0_1/CLKOUT/CT32B0_MAT2/USB_FTOGGLE

JP406 (2-1)	EVG0_GPIO40
JP406 (2-3) (Default)	User LED1

Selecting JP406 position 2-3 allows use of the on board user led LED1 (D401).
Note: EVG0_GPIO40 is also available on JP407. (PIO1_10)

PIO0_2/SSEL/CT16B0_CAP0

JP417 (2-1)	MOTORP2H
JP417 (2-3) (Default)	EVG17_GPIO65

PIO0_3/USB_VBUS

JP438 (2-3)	GPIO7_I2S_RX_CLK

JP438 (2-1) (Default)	EVM0_GPIO21

PIO0_6/#USB_CONNECT/SCK

JP431 (2-3)	ASC1_RX_TTL
JP431 (2-1) (Default)	EVM8_GPIO53

PIO0_8/MISO/CT16B0_MAT0

JP418 (2-1)	MOTORP2L
JP418 (2-3) (Default)	EVG18_GPIO66

Port PIO1 Options

PIO1_4/AD5/CT32B1_MAT3/WAKEUP

JP403 (2-1) (Default)	AN0
JP403 (2-3)	AN8

PIO1_6/RXD/CT32B0_MAT0

JP440 (2-1) (Default)	ASC0_RX_TTL
JP440 (2-4)	AN6
JP440 (2-3)	AN14

Position 2-1 is the main RS232/UART channel. Incoming logic level receive traffic is routed from the Communication Module.

PIO1_7/TXD/CT32B0_MAT1

JP439 (2-1) (Default)	ASC0_TX_TTL
JP439 (2-4)	AN7
JP439 (2-3)	AN15

Position 2-1 is the main RS232/UART channel. Outgoing logic level transmit traffic is routed to the Communication Module where it is translated into RS232/RS485 logic levels.

PIO1_8/CT16B1_CAP0

JP434 (2-3)	GPIO14_MCI_PWR
JP434 (2-1) (Default)	EVM4_GPIO45

PIO1_9/CT16B1_MAT0

JP437 (2-3)	GPIO9_I2S_RX_WS
JP437 (2-1) (Default)	EVM1_GPIO23
JP437 (2-4)	CPU_DACO0_GPIO17

Note: CPU_DACO0_GPIO17 is also available on JP430 (PIO2_9)

PIO1_10/AD6/CT16B1_MAT1

JP407 (2-1) (Default)	EVG5_GPIO50
JP407 (2-3)	EVG8_GPIO56
JP407 (2-4)	EVG0_GPIO40

Note: EVG0_GPIO40 is also available on JP406. (PIO0_1)

PIO1_11/AD7

JP405 (2-1) (Default)	AN4
JP405 (2-3)	AN12

Port PIO2 Options

PIO2_0/#DTR

JP421 (2-1) (Default)	GPIO0
JP421 (2-3)	EVG6_GPIO52

PIO2_1/#DSR

JP426 (2-1) (Default)	ASC1_TX_TTL_ASC0_DTR
JP426 (2-3)	CAN1_RX

PIO2_2/#DCD

JP428 (2-1) (Default)	EVG4_GPIO48
JP428 (2-3)	EVG19_GPIO67

PIO2_3/#RI

JP411 (2-1)	EMG_TRAP
JP411 (2-3) (Default)	EVG11_GPIO59

PIO2_4

JP435 (2-3)	GPIO12_MCI_CMD
JP435 (2-1) (Default)	EVM3_GPIO43

PIO2_5

JP433 (2-3)	GPIO2_MCI_DAT0
JP433 (2-1) (Default)	EVM6_GPIO49

PIO2_7

JP436 (2-3)	GPIO10_MCI_CLK
JP436 (2-1) (Default)	EVM2_GPIO41_CAPADC

PIO2_8

JP432 (2-3)	ASC1_TX_TTL
JP432 (2-1) (Default)	EVM7_GPIO51

PIO2_9

JP430 (2-3)	CPU_DACO0_GPIO17
JP430 (2-1) (Default)	EVG2_GPIO44

Note: CPU_DACO0_GPIO17 is also available on JP437 (PIO1_9)

PIO2_10

JP429 (2-3)	CPU_DAC01_GPIO19
JP429 (2-1) (Default)	EVG3_GPIO46

PIO2_11/SCK

JP422 (2-1) (Default)	GPIO1

JP422 (2-3)	EVG7_GPIO54

Port PIO3 Options

PIO3_0

JP409 (2-1)	MOTORP0H
JP409 (2-3) (Default)	EVG9_GPIO57

PIO3_1

JP410 (2-1)	MOTORH0_ENC0
JP410 (2-3) (Default)	EVG10_GPIO58

PIO3_2

JP412 (2-1)	MOTORP0L
JP412 (2-3) (Default)	EVG12_GPIO60

PIO3_3

JP413 (2-1)	MOTORH1_ENC1
JP413 (2-3) (Default)	EVG13_GPIO61

Not Connected Options

As the circuit board for the LPC1343 is also used for higher pin count MCU such as LPC2368 and LPC1768, there are some configurations options that are not used. These are shown on the circuit schematic but do not have any relevance for this LPC1343 module as the pins are not connected. These jumper options are detailed below.

JP401 (2-1) (Default)	AN2
JP401 (2-3)	AN10

JP402 (2-1) (Default)	AN1
JP402 (2-3)	AN9

JP404 (2-1) (Default)	AN5
JP404 (2-3)	AN13

JP408 (2-1) (Default)	AN3
JP408 (2-4)	AN11
JP408 (2-3)	CPU_DACO0_GPIO17

JP414 (2-1)	MOTORH2_ENC2
JP414 (2-3) (Default)	EVG14_GPIO62

JP415 (2-1)	MOTORP1H
JP415 (2-3) (Default)	EVG15_GPIO63

JP416 (2-1)	MOTORP1L
JP416 (2-3) (Default)	EVG16_GPIO64

JP419 (2-1)	CAN0_TX
JP419 (2-4) (Default)	CAN0_TX_LOCAL
JP419 (2-3)	I2C_GEN0_SDA

JP420 (2-1)	CAN0_RX
JP420 (2-4) (Default)	CAN0_RX_LOCAL
JP420 (2-3)	I2C_GEN0_SCL

JP423 (2-1) (Default)	IRQ_GPIO16_CNTRL_I2C_INT
JP423 (2-3)	IRQ_GPIO18_I2C_GEN0_INT

JP424 (2-1) (Default)	ASC1_RX_TTL
JP424 (2-3)	EVM10_GPIO68_ASCO_CTS

JP425 (2-1) (Default)	ASC1_TX_TTL
JP425 (2-3)	CAN1_TX

JP427 (2-1)	MOTOR_TCO_FB
JP427 (2-3) (Default)	User LED0

4. Zero Ohm Links

CAN Load Resistor

JP501	This link when inserted includes a 120 ohm resistor across CANH0 and CANL0. The default is connected.

This option is irrelevant as the LPC1343 does not a CAN peripheral. This jumper is provided for the LPC1768/LPC2368 variants of the Command Module, which have a CAN transceiver fitted.

AN_REF

R101	This zero ohm link when inserted provides a 3.3V reference for the EDP platform. The 3.3V used is the local supply voltage derived from a local voltage regulator. This link should be used in the absence of a 3.3V voltage reference voltage provided by the Analogue Module when fitted. The default position is not connected.

AGND & VAGND

R102	This link when inserted provides a way of connecting the VAGND to the SGND. This is the default position. The two grounds alternatively can be connected to each other on the analogue module.

5. Software Support

The NXP Command Module for the RS-EDP platform is supported by all of the necessary software drivers to make driving of the platform very easy. All the low level support for the devices controlled by I2C for example have been written, as well as a test menu to exercise each of the modules independently of the others. This therefore provides working example of the code which will allow students and users to cut and paste various sections into their own applications.

Each Applications Module has its own collection of header files, which provides the support for the functions that control it. Each module has its own set of high level functions that can be called to operate and control the hardware. This makes life a lot easier for the user, who can then spend most of his time working at the higher level application layer.

The software has been packed up as several ZIP file which can be downloaded and unpacked. Most of the projects have been written for the Keil uVision environment.

The majority of the applications written use the serial comm. channel ASC0 for outputting data to a terminal emulator. With this in mind a serial terminal emulation program should be used to read traffic outputted from the RS-EDP platform. Hyper Terminal is included in windows as part of the Windows Operating system but this does not work reliability. With this in mind it may be worth looking at other terminal emulator especially if they are to be used with USB-RS232 converters.

The terminal emulator should be set up for
115,200 baud
8 data bits
no stop bit
no parity
No flow control

The default jumper options for JP439 and JP430 should be left in place to ensure serial traffic is routed to the communication module. Always check the software to see if the baud rate has been changed.

Some of the provided software includes...

5.1 RSEDP_Test_Suite

This software exercises the NXP LPC1343 MCU peripherals including the on board ADC, PWM output, input capture, I2C, and I/O. The software also allows you to exercise the basic Application Modules, which are the Communication Module, the Digital I/O Module, and the Analogue Module. A suite of drivers and test menus are provided to fully exercise all the hardware on these boards.

5.2 MC1_Test_Suite

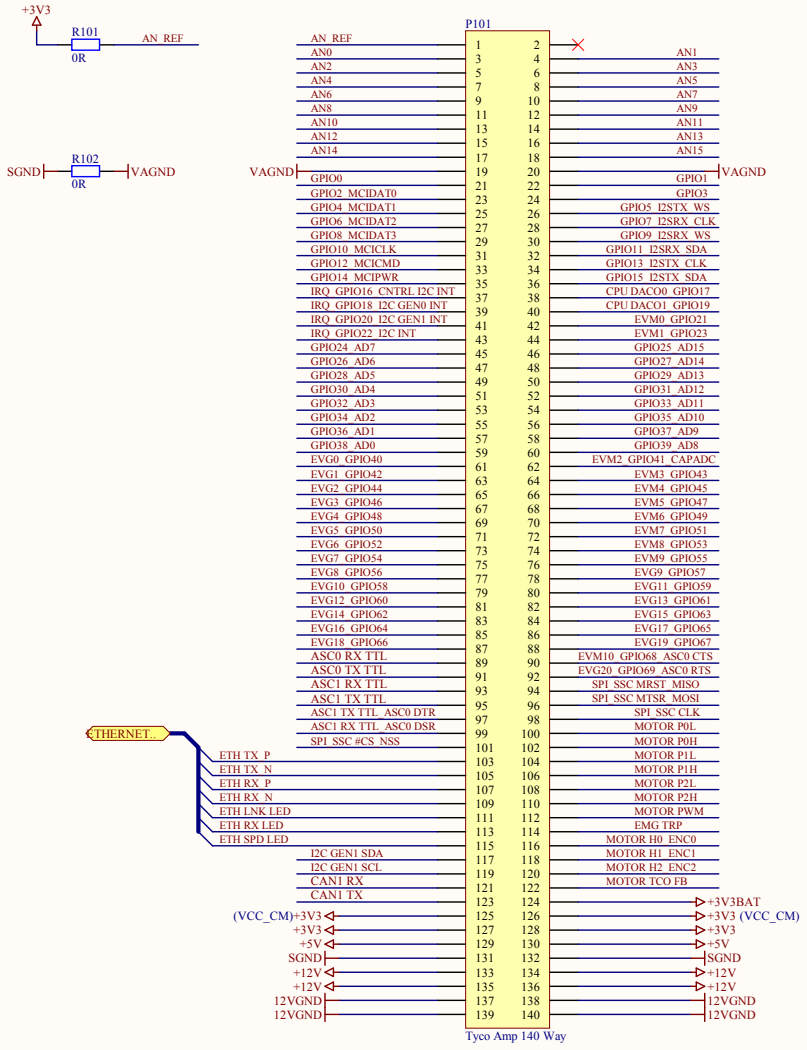
This is similar to the RSEDP_Test_Suite, but the test menus provided are for the MC1 Brushed DC Motor Drive Application Module. The motors are nominally 12V brushed DC motors running in a full H bridge configuration. The test suite allows you to accelerate the motor, change its direction, turn the brake on and off, as well as allowing the monitoring of motor current, DC link voltage and tacho feedback signals. The MC1 motor drive module also has many external inputs for limit switch detection and conditioning of motor related stimuli. The provided software library will therefore allow you to fully exercise your motor.

5.3 MC2_Test_Suite

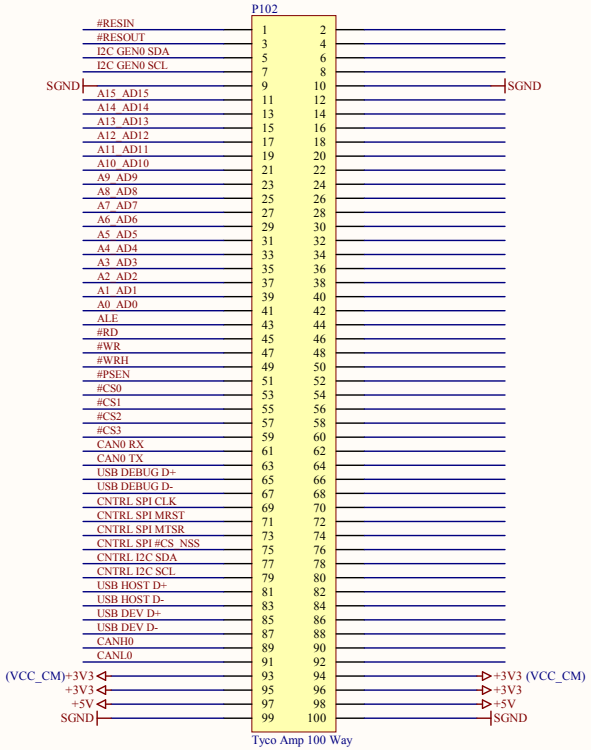
This is similar to the MC1 test suite but for brushless DC/AC motors. The software assumes you have an MC2 motor drive module fitted, and you want to communicate to it via I2C packets. This set of software therefore allows you communicate with the MC2 motor drive module across the I2C backplane network, present in the RSEDP system. You can have up to three MC2 motor drives fitted and this suite of software allows you to communicate with all of them.

Module Position 1

EDPCON1 IO Connector



EDPCON2 Bus/Control Connector



Checked By:	Title: **Module Connectors**		*Hitex (UK) Ltd.* *Sir William Lyons Road* *University of Warwick Science Park* *Coventry*
Approved By:	Size: A3	Number: EDP-CM-LPCx	Revision: B
	Date: 19/03/2010	(c) Hitex (UK) Ltd.	Sheet1 of 5
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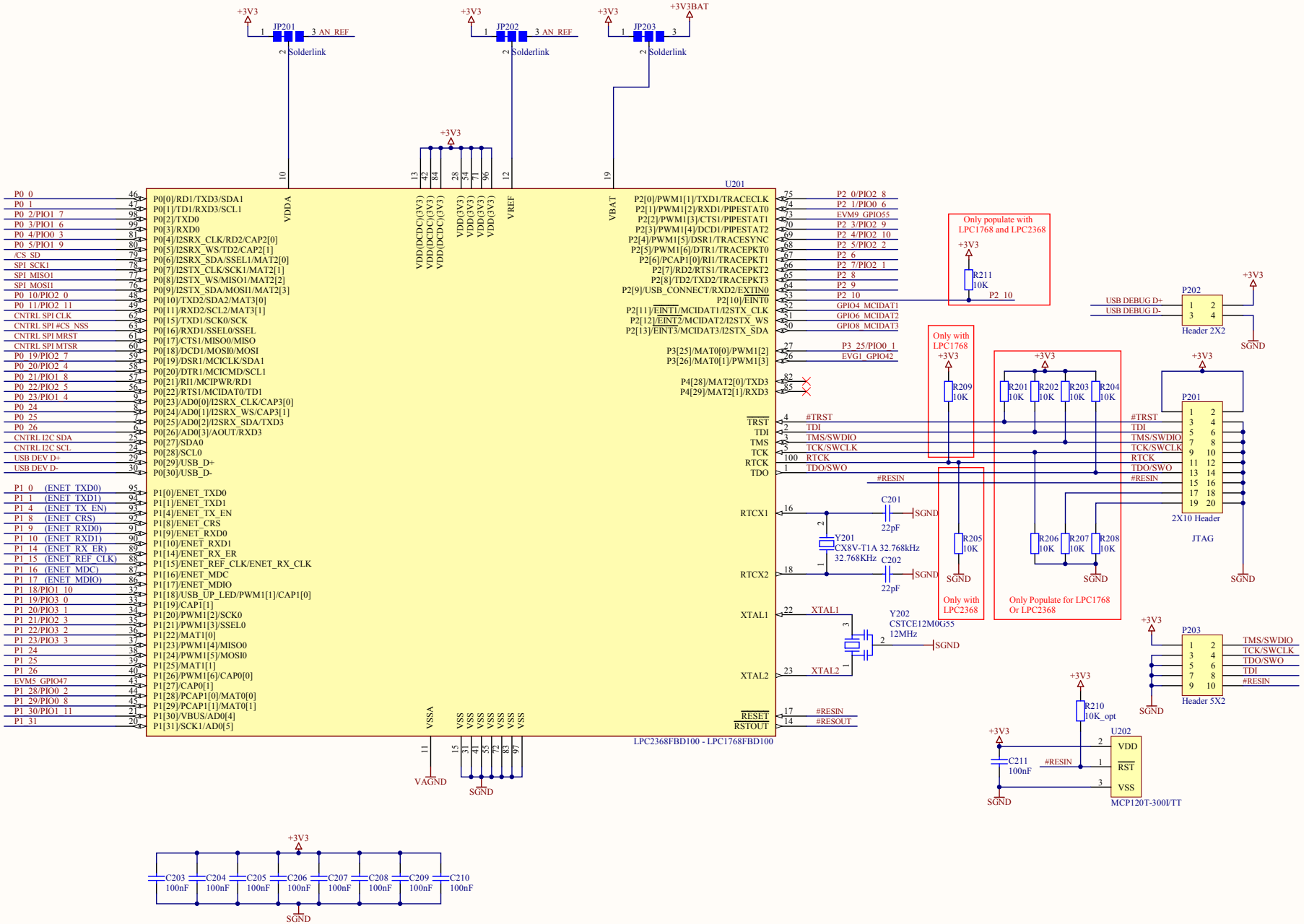

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Approved By:	Size: A3	Number: EDP-CM-LPCx	Revision: B
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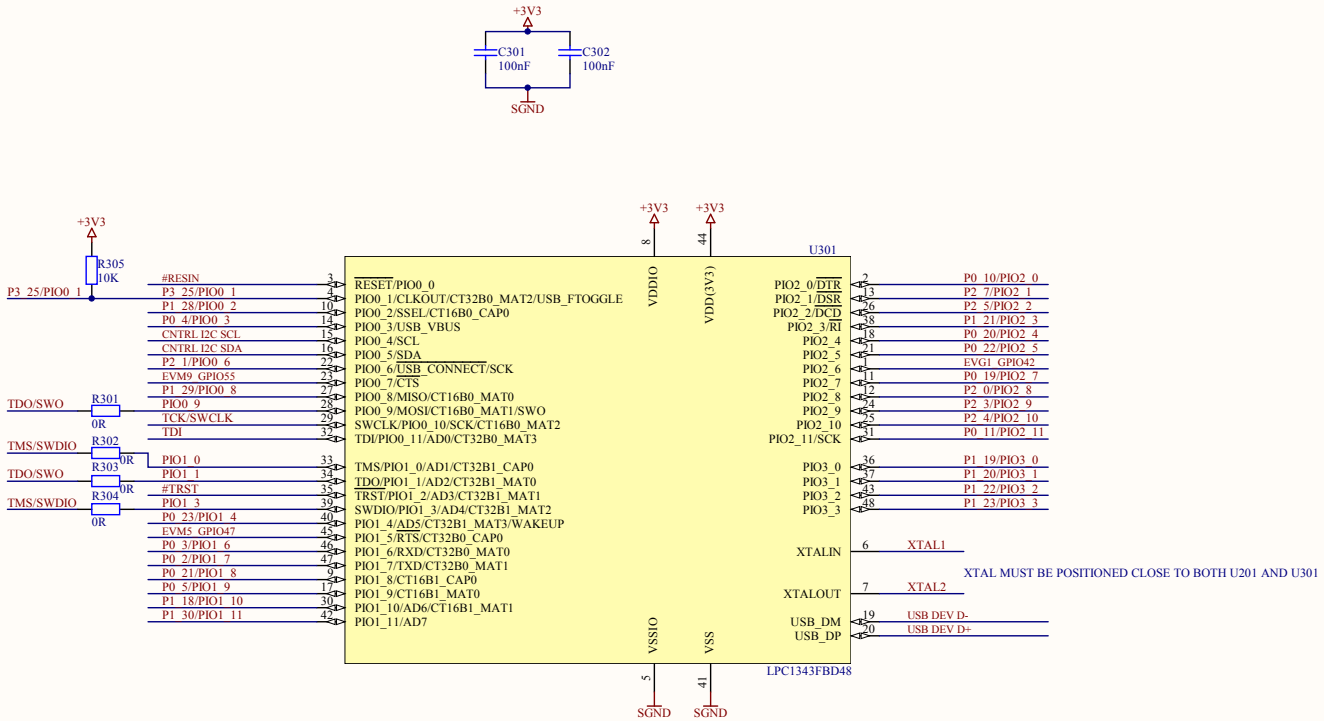

Checked By:	Title: LPC1343		Hitex (UK) Ltd. Sir William Lyons Road University of Warwick Science Park Coventry
Approved By:	Size: A3	Number: EDP-CM-LPC	Revision: B
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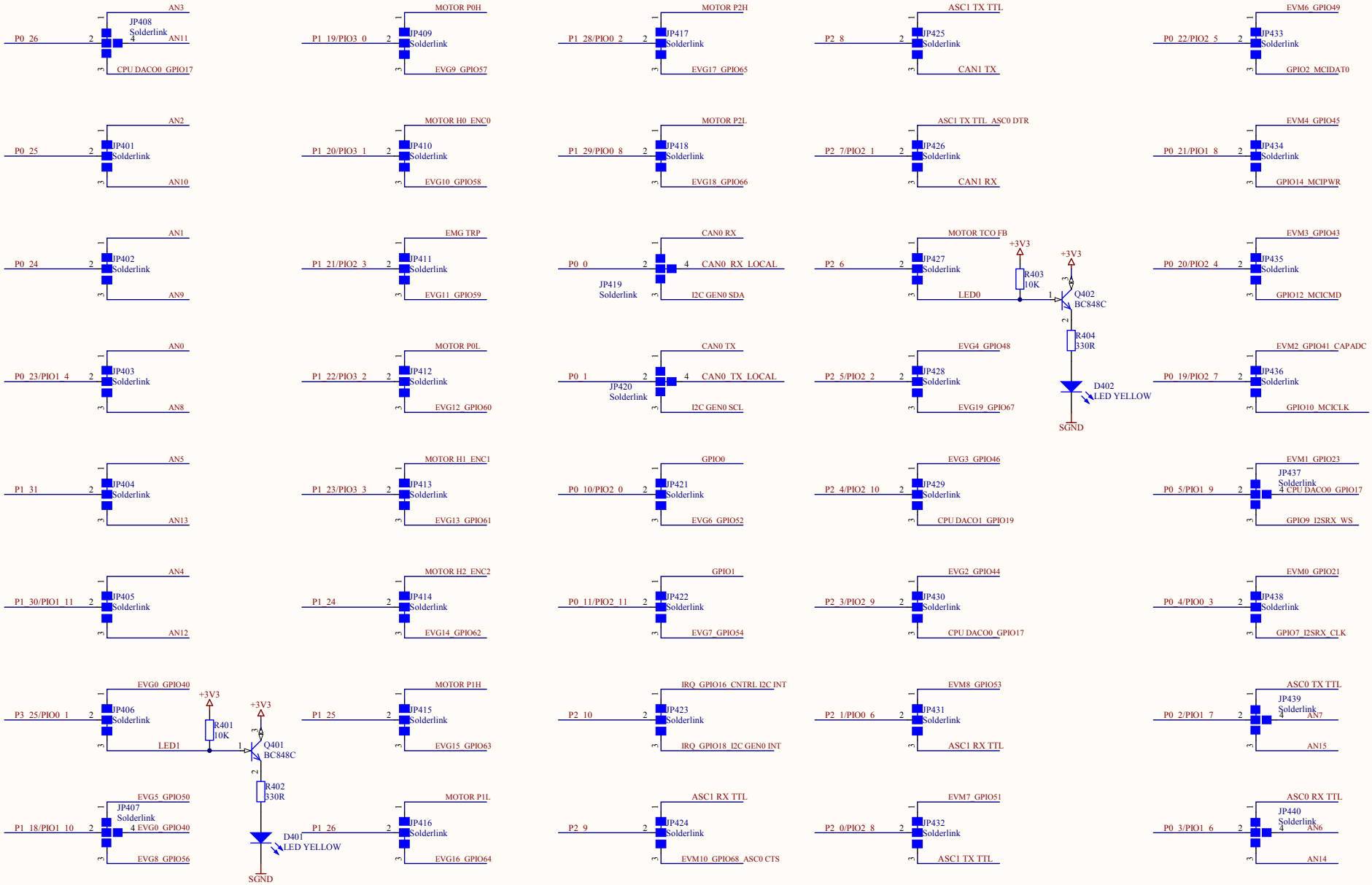
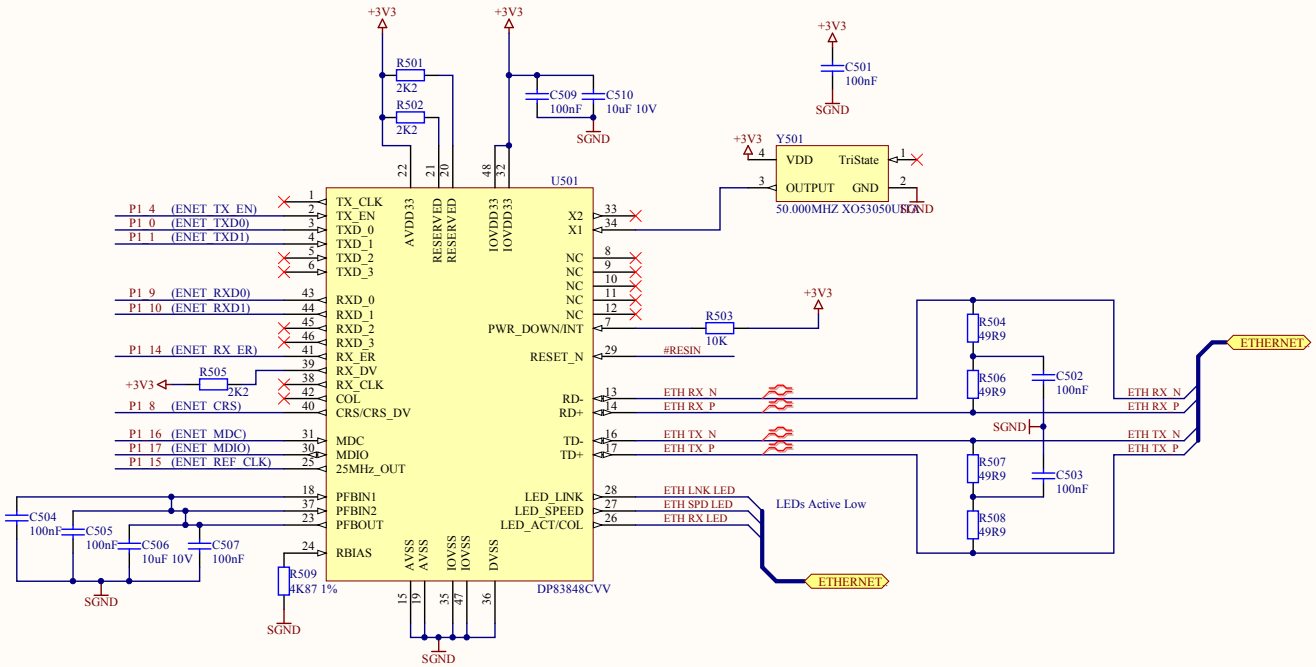
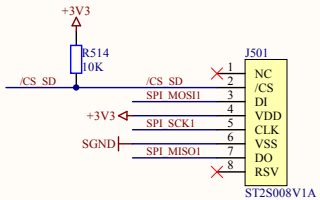
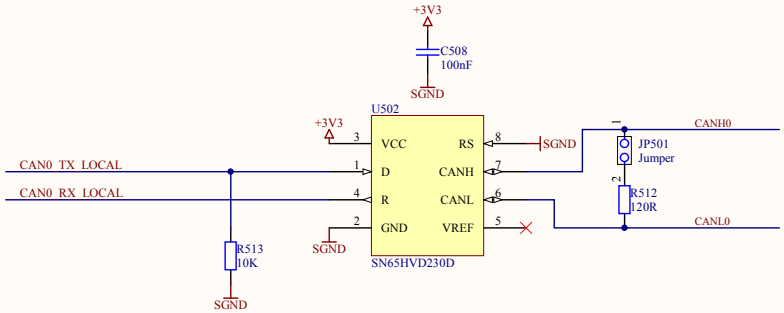


Checked By:	Title: *Link Options*		*Hitex (UK) Ltd.* *Sir William Lyons Road* *University of Warwick Science Park* *Coventry*
Approved By:	Size: A3	Number: EDP-CM-LPC	Revision: B
	Date: 19/03/2010	(c) Hitex (UK) Ltd.	Sheet4 of 5
	File: D:\PCB Designs\DXP\EDP-CM-LPCx\Rev B\Jumpers.SchDoc		Author: A.Davison







Checked By:	Title: *Ethernet, CAN, SD Card*		*Hitex (UK) Ltd.* *Sir William Lyons Road* *University of Warwick Science Park* *Coventry*
Approved By:	Size: A3	Number: EDP-CM-LPCx	Revision: B
	Date: 19/03/2010	(c) Hitex (UK) Ltd.	Sheet5 of 5
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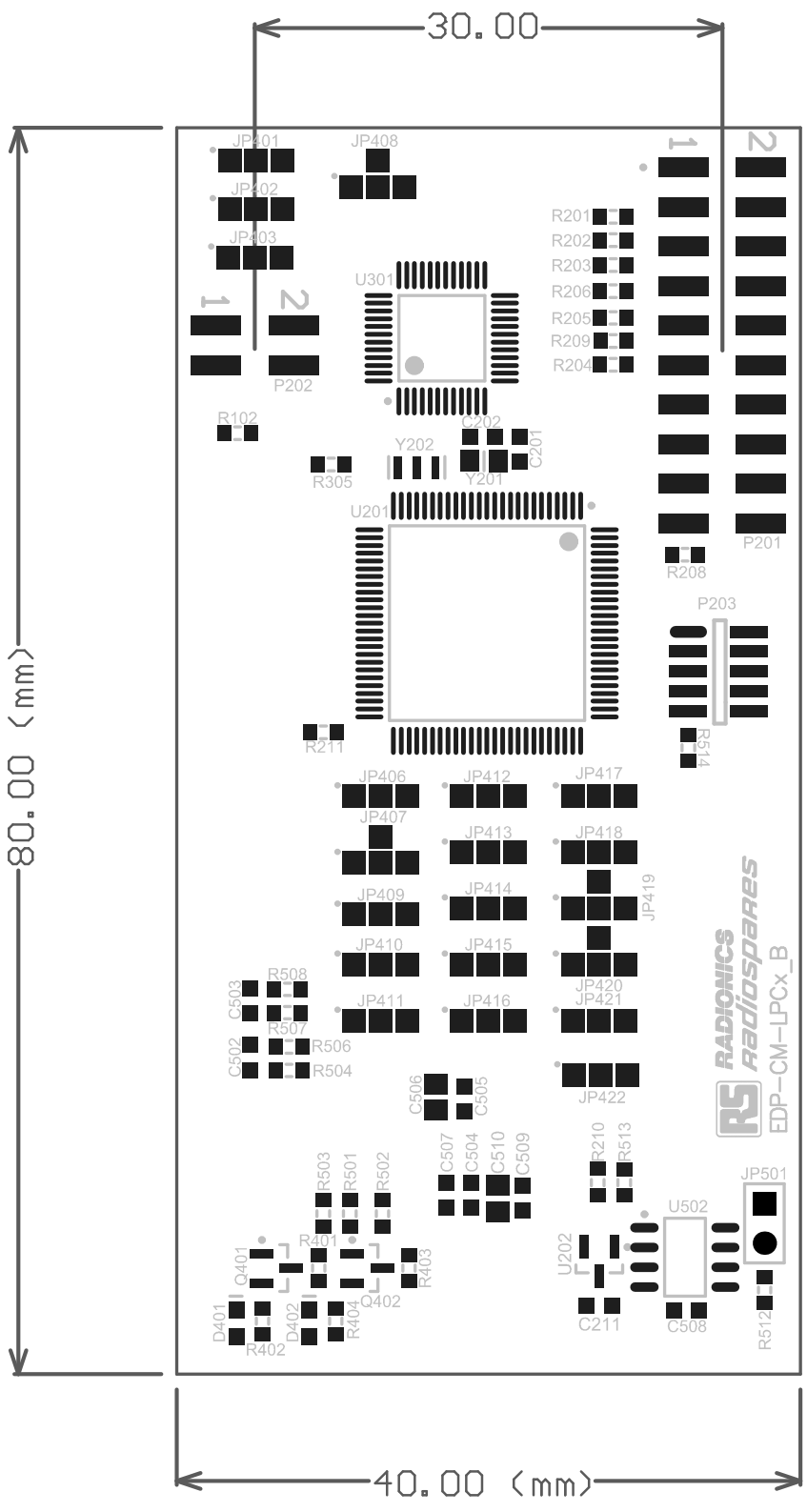
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80.00 (mm)
40.00 (mm)
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JP402
JP403
1
2
P202
U301
R201
R202
R203
R206
R205
R209
R204
R102
C202
Y202
C201
R305
Y201
U201
P201
R208
P203
R211
R514
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RADIONICS
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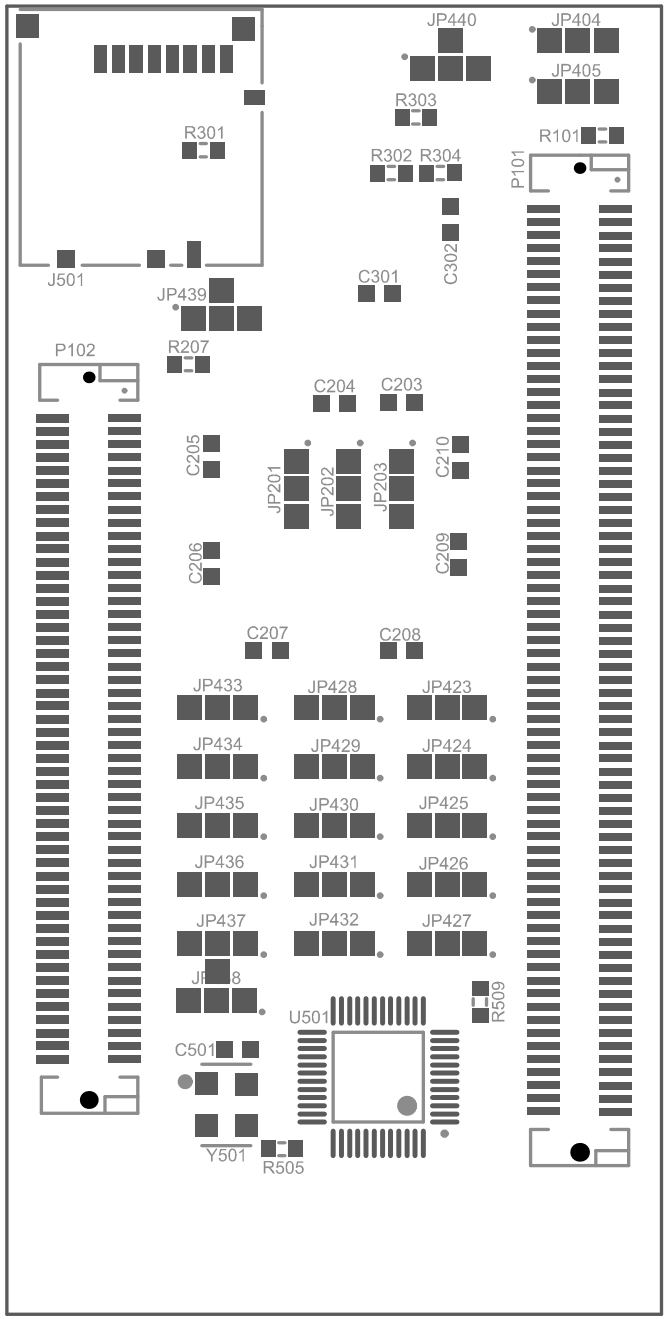
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